CAR0812DC Series DC-DC Converter

Input: -36V_{DC} to -75V_{DC}; Output: +12 V_{DC} @ 850W; 3.3V_{DC} or 5 V_{DC} @ 1A

RoHS Compliant

Applications

- 12V_{DC} distributed power architectures
- Mid-End Servers
- Blade Servers
- Storage Area Networks
- Routers/Switches
- Enterprise Networks
- Advanced workstations

Features

- Reverse input voltage protection
- 2 front panel LEDs: LED 1-input, LED2-[output, fault, over temp]
- Remote ON/OFF control of the 12V_{DC} output
- 12Vdc Regulation: set point ±0.2%, overall ±3%
- 12Vdc programmable between 10.8 – 13.2V_{DC}
- Active load sharing on the 12V output
- Firmware adjustable overload set point of 12V output
- Standby orderable either as 3.3V_{DC} or 5V_{DC}
- Efficiency: typically 92% @ 50% load Exceeds 80plus GOLD standard
- Auto recoverable protection
- Hot insertion/removal (hot plug)
- Operating temperature: -10 - 70°C,
- Digital status & control: I^2C and PMBus+ serial bus
- EN/IEC/UL60950-1 2nd edition; UL*, CSA† and VDE‡
- CE§ mark meets 2006/95/EC directive
- EMI: class B FCC docket 20780 part 15, EN55022
- Meets EN6100 immunity and transient standards

Description

The CAR0812DC series of converters provide highly efficient isolated power from 48/60Vdc -input systems. Offered in the industry standard compact 1U form factor, these converters complement the CAR0812 rectifier line, providing comprehensive solutions for systems connected either to commercial AC mains or 48/60Vdc power plants. This plug and play approach, between AC and DC input units, has significant advantages since systems can be readily reconfigured by simply replacing the power supply.

The high-density, front-to-back airflow is designed for minimal space utilization and is highly expandable for future growth. The industry standard PMBus compliant I^2C communications bus offers a full range of control and monitoring capabilities. The SMBusAlert signal pin alerts customers automatically of any state change within the power supply.

* UL is a registered trademark of Underwriters Laboratories, Inc.
† CSA is a registered trademark of Canadian Standards Association.
‡ VDE is a trademark of Verband Deutscher Elektrotechniker e.V.
§ Intended for integration into end-user equipment. All the required procedures for CE marking of end-user equipment should be followed. (The CE mark is placed on selected products.)
** ISO is a registered trademark of the International Organization of Standards.
\+ PMBus name and logo are registered trademarks of the System Management Interface Forum (SMIF)

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Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only, functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect the device reliability.

Parameter	Symbol	Min	Max	Unit
Input Voltage: Continuous	V_{IN}	+0.3	-75	V_{DC}
Operating Ambient Temperature	T_A	-10	70[1]	°C
Storage Temperature	T_{stg}	-40	85	°C
I/O Isolation voltage (100% factory Hi-Pot tested)			1500	V_{DC}

Electrical Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, load, and temperature conditions.

INPUT

Parameter	Symbol	Min	Typ	Max	Unit
Operational Range	V_{IN}	-36	-48/60	-75	V_{DC}
12V$_{DC}$ output turned OFF	V_{IN}	-32	-33	-35	V_{DC}
12V$_{DC}$ turned ON	V_{IN}	-33	-35	-36	V_{DC}
Maximum Input Current (V_{IN}= -36V$_{DC}$, V_{OUT}= $V_{O, set}$, I_{OUT}=$I_{O, max}$)	I_{IN}			27.1	A_{DC}
Cold Start Inrush Current (Excluding x-caps, 25C, <10ms, per ETSI 300-132)	I_{IN}			40	A_{peak}
Efficiency (T_{AMB}=25°C, V_{IN}=-48V$_{DC}$, V_{OUT}=12V$_{DC}$) 10% load	η		80		%
20% load			88		
50% load			92		
100% load			89		
Holdup time – 12V$_{DC}$(Tamb 25°C, V_{IN} -48V$_{DC}$, C_{ext} 5,000μf)	T	2[2]			ms
Isolation T_{AMB}=25°C, V_{IN}=-48V$_{DC}$, V_{OUT}=12V$_{DC}$ - Input/Output		1500			V_{DC}
Input/Frame		1500			
1 minute per IEC/EN 60950-1) Output/Frame		100			
Ground lug		Connection required to meet EMI performance			

12V$_{dc}$ MAIN OUTPUT

Parameter	Symbol	Min	Typ	Max	Unit
Output power	P_{OUT}	0		850	W_{DC}
Set point	V_{OUT}	11.98	12.00	12.02	V_{DC}
Overall regulation (load, temperature, aging)		-3		+3	%
Ripple and noise[3]				120	mV_{p-p}
Turn-ON overshoot				+3	%
Turn-ON delay	T			2	sec

[1] Derated above 50°C at 2.5%/°C

[2] Full load, with 5,000μf external capacitance, 12Vdc set point, droop to 10.8Vdc permitted, > -48Vdc input

[3] Measured across a 10μf tantalum and a 0.1μf ceramic capacitors in parallel. For V_{in} > 60V$_{dc}$ the PARD is relaxed to 150mV_{p-p}.

12V_{dc} MAIN OUTPUT (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Remote ON/OFF delay time				40	ms
Turn-ON rise time (10 – 90% of V_{out})				50	ms
Transient response 50% step [10%-60%, 50% - 100%] (di/dt – 1A/µs, recovery 500µs)	V_{OUT}	-600		+600	mV_{DC}
Programmable range (hardware & software)	V_{OUT}	10.8		13.2	V_{DC}
Overvoltage protection, latched (recovery by cycling OFF/ON via hardware or software)	V_{OUT}	13.5		15.5	V_{DC}
Output current	I_{OUT}	0		70.8	A_{DC}
Current limit, Hiccup (programmable level)	I_{OUT}	106		126	% of FL
Active current share	I_{OUT}	-5		+5	% of FL
External Capacitance				16,000	µf

STANDBY OUTPUT

Parameter	Symbol	Min	Typ	Max	Unit
Set point	V_{STDBY}		3.3 / 5.0		V_{DC}
Overall regulation (load, temperature, aging)	V_{STDBY}	-5		+5	%
Ripple and noise				50	mV_{p-p}
Output current	I_{STDBY}	0		1	A_{DC}
Transient response: 50% load step (10% - 60%, 50% - 100%, di/dt=1A/µs, recovery 500µs)	V_{STDBY}	-165		165	mV
Overload protection	I_{STDBY}	110		180	% of FL
Isolation Output/Frame		100			V_{DC}

General Specifications

Parameter	Min	Typ	Max	Units	Notes
Reliability		400,000		Hrs	Full load, 25°C ; MTBF per SR232 Reliability protection for electronic equipment, method I, case III,
Service Life		10		Yrs	Full load, excluding fans
Weight		1.09 (2.4)		Kgs (Lbs)	

Feature Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions. See Feature Descriptions for additional information.

Parameter	Symbol	Min	Typ	Max	Unit
Remote ON/OFF (pulled up internally within the module)					
Logic High (Module ON)		0.7V_{STDBY}		V_{STDBY}	V_{DC}
Logic Low (Module OFF)	I_{IL}	—	—	1	mA
	V_{IL}	0	—	0.8	V_{DC}

Feature Specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltage programming (Vprog)					
Equation: V_{OUT} = 10.8 + (Vprog * 0.96)					
Vprog range	V_{prog}	0	—	2.5	V_{DC}
Programmed output voltage range	V_{OUT}	10.8	—	13.2	V_{DC}
Voltage adjustment resolution (8-bit A/D)	V_{OUT}	—	10	—	mV_{DC}
Output configured to 13.2V_{DC}	V_{prog}	2.5		3.0	V_{DC}
Output configured to the 12V_{DC} set-point	V_{prog}	3.0	—	—	V_{DC}
Enable [short pin controlling presence of the 12V_{DC} output]					
12V output OFF	V_I	0.7V_{DD}	—	12	V_{DC}
12V output ON	V_I	0	—	0.8	V_{DC}
Write protect (Wp)					
Write protect enabled	V_I	0.7V_{DD}	—	12	V_{DC}
Write protect disabled	V_I	0	—	0.8	V_{DC}
INPUT-OK (Needs to be pulled HI via an external resistor)					
Logic High (Input within normal range)	I_{OH}		—	20	μA
	V_{OH}	0.7V_{DD}	—	12	V_{DC}
Logic Low (Input out of range)	I_{OL}	—	—	4	mA
	V_{OL}	0	—	0.4	V_{DC}
DC-OK (Internally connected to 3.3V via a 10kΩ resistor)					
Logic High (Output voltage is present)	I_{OH}		—	20	μA
	V_{OH}	0.7V_{DD}	—	12	V_{DC}
Logic Low (Output voltage is not present)	I_{OL}	—	—	4	mA
	V_{OL}	0	—	0.4	V_{DC}
Over Temperature Warning (Needs to be pulled HI via an external					
Logic High (temperature within normal range)	I_{OH}		—	20	μA
	V_{OH}	0.7V_{DD}	—	12	V_{DC}
Logic Low (temperature is too high)	I_{OL}	—	—	4	mA
	V_{OL}	0	—	0.4	V_{DC}
Delayed shutdown after Logic Low transition	Tdelay	10			sec
Fault (Needs to be pulled HI via an external resistor)					
Logic High (No fault is present)	I_{OH}		—	20	μA
	V_{OH}	0.7V_{DD}	—	12	V_{DC}
Logic Low (Fault is present)	I_{OL}	—	—	4	mA
	V_{OL}	0	—	0.4	V_{DC}
PS Present (Needs to be pulled HI via an external resistor)					
Logic High (Power supply is not plugged in)					
Logic Low (Power supply is present)	V_{IL}	0	—	0.1	V_{DC}

Feature Specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit
SMBAlert# (Interrupt) (Needs to be pulled HI via an external					
Logic High (No Alert - normal)	I_{OH}		—	20	µA
	V_{OH}	0.7V_{DD}	—	12	V_{DC}
Logic Low (Alert is set)	I_{OL}	—	—	4	mA
	V_{OL}	0	—	0.4	V_{DC}
Output current monitor (Imon)					
Resolution			40		mV/A
Measurement range	I_{OUT}	0		80	A_{DC}
Analog output range	V_{mon}	0		3	V_{DC}
Sourced output current	I_{OUT}			5	mA_{DC}

Digital Interface Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
PMBus Signal Interface Characteristics						
Input Logic High Voltage (CLK, DATA)		V_{IH}	2.1		3.6	V_{DC}
Input Logic Low Voltage (CLK, DATA)		V_{IL}	0		0.8	V_{DC}
Input high sourced current (CLK, DATA)		I_{IH}	0		10	µA
Output Low sink Voltage (CLK, DATA, SMBALERT#)	I_{OUT}=3.5mA	V_{OL}			0.4	V_{DC}
Output Low sink current (CLK, DATA, SMBALERT#)		I_{OL}	3.5			mA
Output High open drain leakage current (CLK,DATA, SMBALERT#)	V_{OUT}=3.6V	I_{OH}	0		10	µA
PMBus Operating frequency range	Slave Mode	F_{PMB}	10		400	kHz
Measurement System Characteristics (all measurement tolerances are typical estimations under normal operating conditions)						
Clock stretching		$t_{STRETCH}$			25	ms
I_{OUT} measurement range	Linear	I_{RNG}	0		80	A_{DC}
I_{OUT} measurement accuracy 25°C		I_{ACC}	-3		+3	% of FL
V_{OUT} measurement range	Linear	$V_{OUT(rng)}$	0		14	V_{DC}
V_{OUT} measurement accuracy		$V_{OUT(acc)}$	-3		+3	%
Temp measurement range	Linear	$Temp_{(rng)}$	0		120	°C
Temp measurement accuracy[4]		$Temp_{(acc)}$	-5		+5	°C
V_{IN} measurement range	Linear	$V_{IN(rng)}$	0		80	V_{DC}
V_{IN} measurement accuracy		$V_{IN(acc)}$	-3		+3	%
Fan Speed measurement range	Linear		0		30k	RPM
Fan Speed measurement accuracy			-5		5	%
Fan speed control range	-direct-		0		100	%

[4] Temperature accuracy reduces non-linearly with decreasing temperature

Environmental Specifications

Parameter	Min	Typ	Max	Units	Notes
Ambient Temperature	-10[5]		70	°C	Derated above 50°C
Storage Temperature	-40		85	°C	
Operating Altitude			2250/7382	m/ft	
Non-operating Altitude			8200/30k	m / ft	
Power Derating with Temperature			2.5	%/°C	50°C to 70°C
Power Derating with Altitude			2.0	°C/301 m °C/1000 ft	Above 2250 m/7382 ft
Acoustic noise			55	dbA	Full load
Over Temperature Protection		125/110		°C	Shutdown / restart
Humidity Operating Storage	 30 10		 95 95	%	Relative humidity, non-condensing
Shock and Vibration acceleration			7.7	Grms	NEBS GR-63-CORE, Level 3, 20 - 2000Hz, min 30 minutes
Earthquake Rating	4			Zone	NEBS GR-63-CORE, all floors, Seismic Zone 4 Designed and tested to meet NEBS specifications.

EMC Compliance

Parameter	Criteria	Standard	Level	Test
DC input	Conducted emissions	EN55022, FCC Docket 20780 part 15, subpart J	B	0.15 – 30MHz
	Radiated emissions[6]	EN55022	B	30 – 10000MHz
DC Input Immunity	Fast transients	EN61000-4-4	B	5/50ns, 1kV
Enclosure immunity	Conducted RF fields	EN61000-4-6	A	130dBµV, 0.15-80MHz, 80% AM
	Radiated RF fields	EN61000-4-3	A	10V/m, 80-1000MHz, 80% AM
	ESD	EN61000-4-2	B	4kV contact, 8kV air

[5] Designed to start at an ambient down to -40°C; meet spec after ≅ 30 min warm up period, may not meet operational limits below -10°C.
[6] Radiated emissions compliance is contingent upon the final system configuration.

Characteristic Curves

The following figures provide typical characteristics for the CAR0812DC converter at 25°C

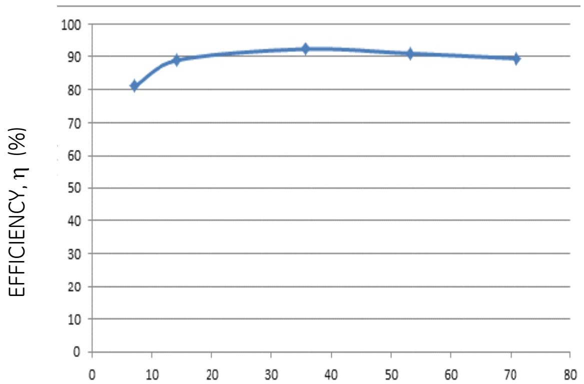


Figure 1. Converter Efficiency versus Output Current.

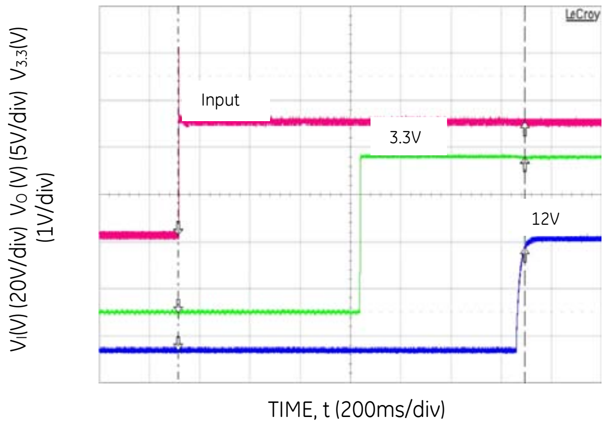


Figure 2. Input start up (Vin: -48V$_{DC}$, full load).

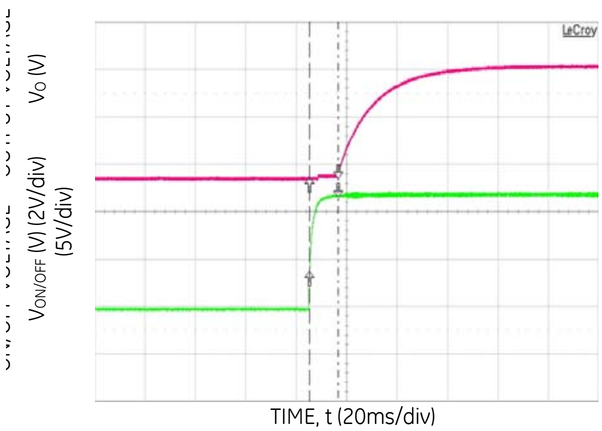


Figure 3. Start-up Using Remote On/Off (Vin: -48V$_{DC}$, load independent)

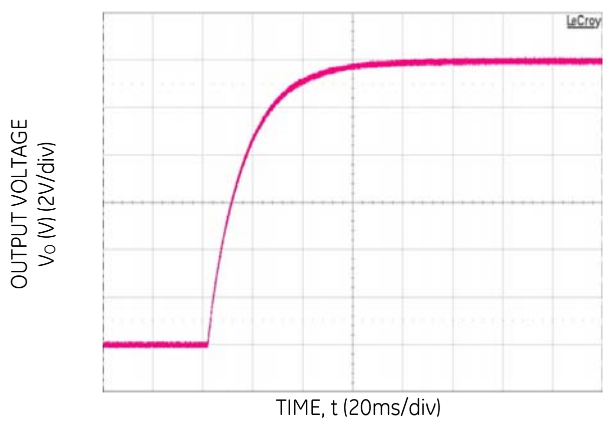


Figure 4. 12V start-up with 16,000µf external capacitance (Vin: -48V$_{DC}$, full load)

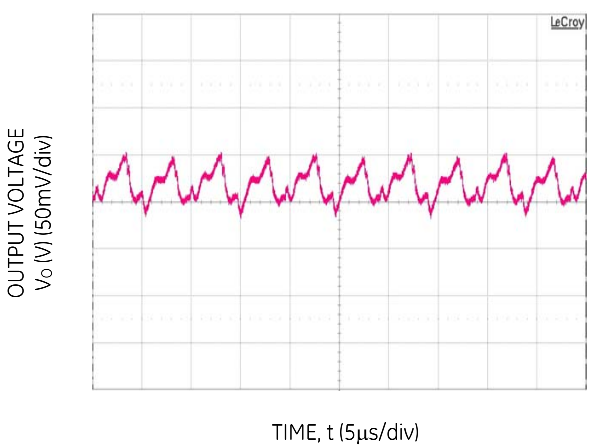


Figure 5. 12V output ripple and noise (Vin: -48V$_{DC}$, full load).

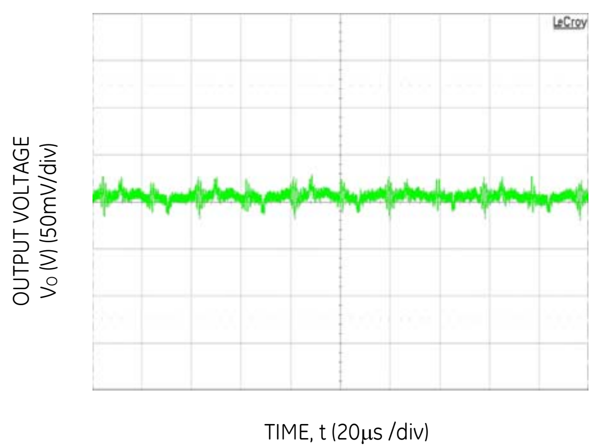


Figure 6. 3.3V output ripple and noise (Vin: -48V$_{DC}$, full load).

Characteristic Curves (continued)

The following figures provide typical characteristics for the CAR0812DC converter at 25°C

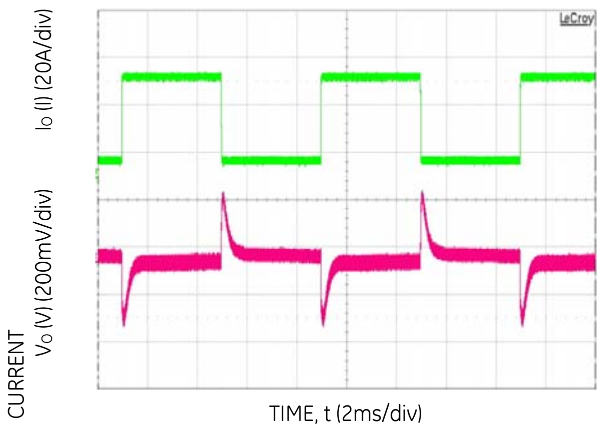


Figure 7. 12V transient response for 10 to 60% step load, Vin: -48V$_{DC}$, slew rate 1A/µs.

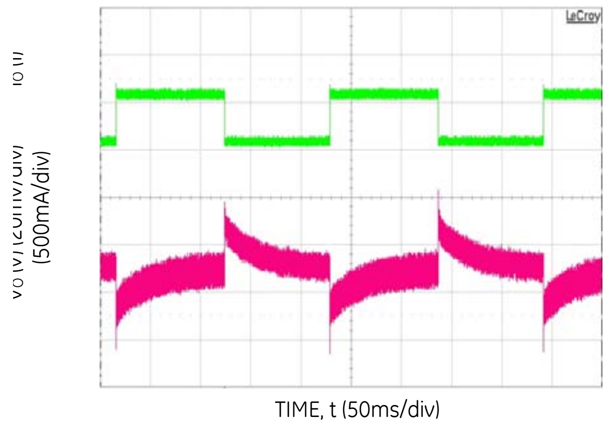


Figure 7. 12V transient response for 10 to 60% step load, Vin: -48V$_{DC}$, slew rate 1A/µs.

Vout	Iout	Iout Total (A)	Iout unit #1 (A)	Iout unit #2 (A)	Ishare
11.968	25%	35.47	18.54	16.93	1.13%
11.96	30%	42.51	22.07	20.44	1.15%
11.923	50%	70.4	36.09	34.31	1.25%
11.877	75%	106	54.25	51.75	1.76%
11.831	100%	140.86	71.65	69.21	1.72%

Vin = 48Vdc

Table 9. Current share accuracy among two CAR0812DC units

Vout	Iout	Iout Total (A)	Iout DC unit (A)	Iout AC unit (A)	Ishare
11.972	25%	35.32	17.71	17.61	0.07%
11.965	30%	42.4	21.43	20.97	0.32%
11.925	50%	69.91	34.07	35.84	1.25%
11.878	75%	104.74	50.81	53.93	2.20%
11.831	100%	140.09	68.99	71.1	1.49%

Vin = 48Vdc

Table 10. Current share accuracy among a CAR0812AC and a CAR0812DC unit

	NO LOAD		
	(-10°C)	25°C	50°C
Turn ON point (V)	35	34.9	34.9
Turn OFF point (V)	32.7	32.7	32.7
Hysteresis (V)	2.3	2.2	2.2

Table 11. Input under voltage protection – no load

	FULL LOAD		
	(-10°C)	25°C	50°C
Turn ON point (V)	35.8	35.6	35.5
Turn OFF point (V)	33.3	33.5	33.4
Hysteresis (V)	2.5	2.1	2.1

Table 12. Input under voltage protection – full load

	RT3 (actual temperature)
Full load 50°C ambient	75°C
Half load 70°C ambient	79.1°C
Protect point	95°C
Recovery point	79°C

Table 13. Over-temperature protection; Actual temperature readings and protection levels.

Control and Status

Control hierarchy: Some features, such as output voltage, can be controlled both through hardware and firmware. For example, the output voltage is controlled both by the signal pin (Vprog) and the PMBus command, (Vout_command) .

Using output voltage as an example; the Vprog signal pin has ultimate control of the output voltage until the Vprog is either > 3Vdc or a no connect. When the programming signal via Vprog is either a no connect or > 3Vdc, it is ignored, the output voltage is set at its nominal 12Vdc and the unit output voltage can be controlled via the PMBus command, (Vout_command).

Analog controls: Details of analog controls are provided in this data sheet under Signal Definitions.

Common ground: All signals and outputs are referenced to Output return. These include 'Vstb return' and 'Signal return'.

Control Signals

Voltage programming (Vprog): An analog voltage on this signal can vary the output voltage ± 10% of nominal, from 10.8V$_{DC}$ to 13.2V$_{DC}$. The equation of this signal is:

$V_{OUT} = 10.8 \div (Vprog * 0.96)$ where Vprog = 0 to 2.5V$_{DC}$

Between 2.5 and 3V the output stays at 13.2V$_{DC}$. If Vprog is > 3V, or left open, the programming signal is ignored and the unit output is set at the setpoint of 12V$_{DC}$.

Load share (Ishare): This is a single wire analog signal that is generated and acted upon automatically by power supplies connected in parallel. The Ishare pins should be tied together for power supplies if active current share among the power supplies is desired. No resistors or capacitors should get connected to this pin.

Remote_ON/OFF: Controls presence of the 12V$_{DC}$ output voltage. A logic LO on this signal pin turns OFF the 12V$_{DC}$ output.

Enable: This is a short signal pin that controls the presence of the 12Vdc main output. This pin should be connected to 'output return' on the system side of the output connector. The purpose of this pin is to ensure that the output turns ON after engagement of the power blades and turns OFF prior to disengagement of the power blades.

Write protect (WP): This signal protects the contents of the EEPROM from accidental over writing. When left open the EEPROM is write protected. A LO (TTL compatible) permits writing to the EEPROM. This signal is pulled HI internally by the power supply.

Status Signals

Output current monitor (Imon): A voltage level proportional to the delivered output current is present on this pin. The signal level is 0.04V per amp ± 0.25V.

Input_OK: A TTL compatible status signal representing whether the input voltage is within the anticipated range. This signal needs to be pulled HI externally through a resistor.

DC_OK: A TTL compatible status signal representing whether the output voltage is present. This signal needs to be pulled HI externally through a resistor.

Over_temp_warning: A TTL compatible status signal representing whether an over temperature exists. This signal needs to be pulled HI externally through a resistor.

If an over temperature should occur, this signal would pull LO for approximately 10 seconds prior to shutting down the power supply. The unit would restart if internal temperatures recover within normal operational levels. At that time the signal reverts back to its open collector (HI) state.

Fault: A TTL compatible status signal representing whether a Fault occurred. This signal needs to be pulled HI externally through a resistor.

This signal activates for OTP, OVP, OCP, INPUT fault or No output.

PS_Present: This pin is connected to 'output return' within the power supply. Its intent is to indicate to the system that a power supply is present. This signal may need to be pulled HI externally through a resistor.

Interrupt (SMBAlert): A TTL compatible status signal, representing the SMBusAlert# feature of the PMBus compatible i²C protocol in the power supply. This signal needs to be pulled HI externally through a resistor.

Serial Bus Communications

The I²C interface facilitates the monitoring and control of various operating parameters within the unit and transmits these on demand over an industry standard I²C Serial bus.

All signals are referenced to 'Signal Return'.

Device addressing: The microcontroller (MCU) and the EEPROM have the following addresses:

Device	Address	Address Bit Assignments (Most to Least Significant)							
MCU	0xBx	1	0	1	1	A2	A1	A0	R/W
Broadcast	0x00	0	0	0	0	0	0	0	0
EEPROM	0xAx	1	0	1	0	A2	A1	A0	R/W

The **Global Broadcast** instruction executes a simultaneous ***write*** instruction to all power supplies. A ***read*** instruction cannot be accessed globally. The three programmable address bits are the same for all I²C accessible devices within the power supply.

Address lines (A2, A1, A0): These signal pins allow up to eight (8) modules to be addressed on a single I²C bus. The pins are pulled HI internal to the power supply. For a logic LO these pins should be connected to 'Output Return'

Serial Clock (SCL): The clock pulses on this line are generated by the host that initiates communications across the I²C Serial bus. This signal is pulled up internally to 3.3V by a 10kΩ resistor. The end user should add additional pull up resistance as necessary to ensure that rise and fall time timing and the maximum sink current is in compliance to the I²C specifications.

Serial Data (SDA): This line is a bi-directional data line. . This signal is pulled up internally to 3.3V by a 10kΩ resistor. The end user should add additional pull up resistance as necessary to ensure that rise and fall time timing and the maximum sink current is in compliance to the I²C specifications.

Digital Feature Descriptions

PMBus™ compliance: The power supply is fully compliant to the Power Management Bus (PMBus™) rev1.2 requirements.

Manufacturer specific commands located between addresses 0xD0 to 0xEF provide instructions that either do not exist in the general PMBus specification or make the communication interface simpler and more efficient.

Master/Slave: The 'host controller' is always the MASTER. Power supplies are always SLAVES. SLAVES cannot initiate communications or toggle the Clock. SLAVES also must respond expeditiously at the command of the MASTER as required by the clock pulses generated by the MASTER.

Clock stretching: The 'slave' µController inside the power supply may initiate clock stretching if it is busy and it desires to delay the initiation of any further communications. During the clock stretch the 'slave' may keep the clock LO until it is ready to receive further instructions from the host controller. The maximum clock stretch interval is 25ms.

The host controller needs to recognize this clock stretching, and refrain from issuing the next clock signal, until the clock line is released, or it needs to delay the next clock pulse beyond the clock stretch interval of the power supply.

Note that clock stretching can only be performed after completion of transmission of the 9th ACK bit, the exception being the START command.

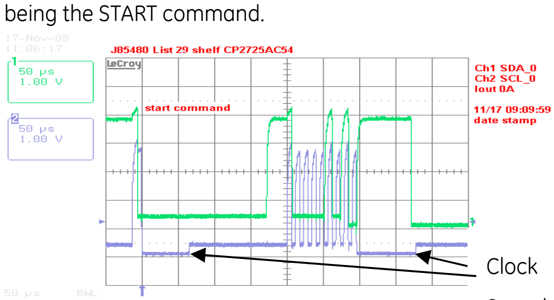


Figure 14. Example waveforms showing clock s

I²C Bus Lock-Up detection: The device will abort any transaction and drop off the bus if it detects the bus being held low for more than 35ms.

Communications speed: Both 100kHz and 400kHz clock rates are supported. The power supplies default to the 100kHz clock rate. The minimum clock speed specified by SMBus is 10 kHz.

Packet Error Checking (PEC): Although the power supply will respond to commands with or without the trailing PEC, it is highly recommended that PEC be used in all communications. The integrity of communications is compromised if packet error correction is not employed. There are many functional features, including turning OFF the main output, that should require validation to ensure that the correct command is executed.

PEC is a CRC-8 error-checking byte, based on the polynomial $C(x) = x^8 + x^2 + x + 1$, in compliance with PMBus™ requirements. The calculation is based in all message bytes, including the originating write address and command bytes preceding read instructions. The PEC is appended to the message by the device that supplied the last byte.

SMBAlert#: The µC driven SMBAlert# signal informs the 'master/host' controller that either a STATE or ALARM change has occurred. Normally this signal is HI. The signal will change to its LO level if the power supply has changed states and the signal will be latched LO until the power supply either receives a 'clear' instruction as outlined below or executes a READ STATUS_WORD. If the alarm state is still present after the STATUS registers were reset, then the signal will revert back into its LO state again and will latch until a subsequent reset signal is received from the host controller.

The signal will be triggered for any state change, including the following conditions;

- VIN under or over voltage
- Vout under or over voltage
- IOUT over current
- Over Temperature warning or fault
- Fan Failure
- Communication error
- PEC error
- Invalid command
- Internal faults

The power supply will clear the SMBusAlert# signal (release the signal to its HI state) upon the following events:

- Receiving a CLEAR_FAULTS command
- The main output recycled (turned OFF and then ON) via the ENABLE signal pin
- The main output recycled (turned OFF and then ON) by the OPERATION command
- Execution of a READ of the STATUS_WORD register

Global broadcast: This is a powerful command because it can instruct all power supplies to respond simultaneously in one command. But it does have a serious disadvantage. Only a single power supply needs to pull down the ninth *acknowledge* bit. To be certain that each power supply responded to the global instruction, a *READ* instruction should be executed to each power supply to verify that the command properly executed. The GLOBAL BROADCAST command should only be executed for write instructions to slave devices.

Read back delay: The power supply issues the SMBAlert # notification as soon as the first state change occurred. During an event a number of different states can be transitioned to before the final event occurs. If a read back is implemented rapidly by the host a successive SMBAlert# could be triggered by the transitioning state of the power supply. In order to avoid the triggering of successive SMBAlert# s and thus reading a transitioning state, it is prudent to wait more than 2 seconds after the receipt of an SMBAlert# before executing a read back. This delay will ensure that only the final state of the power supply is captured.

Successive read backs: Successive read backs to the power supply should not be attempted at intervals faster than every one second. This time interval is sufficient for the internal processors to update their data base so that successive reads provide fresh data.

PMBus™ Commands

Standard instruction: Up to two bytes of data may follow an instruction depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is optional and includes the address and data fields.

1	8		1	8	1
S	Slave address	Wr	A	Command Code	A

8	1	8	1	8	1	1
Low data byte	A	High data byte	A	PEC	A	P

Master to Slave / Slave to Master

SMBUS annotations; S – Start , Wr – Write, Sr – re-Start, Rd – Read,

A – Acknowledge, NA – not-acknowledged, P – Stop

Standard READ: Up to two bytes of data may follow a READ request depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields. PEC is optional and includes the address and data fields.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

1	7	1	1	8	1
Sr	Slave Address	Rd	A	LSB	A

8	1	8	1	1
MSB	A	PEC	No-ack	P

Block instruction: When writing or reading more than two bytes of data at a time BLOCK instructions for WRITE and READ commands must be used instead of the Standard Instructions.

Block write format:

1	7	1	1		8	1
S	Slave address	Wr	A		Command Code	A

8	1	8	1	8		1
Byte count = N	A	Data 1	A	Data 2		A

8	1	8	1	8	1	1
....	A	Data 48	A	PEC	A	P

Block read format:

1	7	1	1		8	1
S	Slave address	Wr	A		Command Code	A

1	7	1	1
Sr	Slave Address	Rd	A

8	1	8	1	8		1
Byte count = N	A	Data 1	A	Data 2		A

8	1	8	1	8	1	1
....	A	Data 48	A	PEC	NoAck	P

Linear Data Format The definition is identical to Part II of the PMBus Specification. All standard PMBus values, with the exception of output voltage related functions, are represented by the linear format described below. Output voltage functions are represented by a 16 bit mantissa. Output voltage has a E=9 constant exponent.

The Linear Data Format is a two byte value with an 11-bit, two's complement mantissa and a 5-bit, two's complement exponent or scaling factor, its format is shown below.

	Data Byte High								Data Byte Low							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Exponent (E)					Mantissa (M)										

The relationship between the Mantissa, Exponent, and Actual Value (V) is given by the following equation:

$$V = M * 2^E$$

Where:

V is the value

M is the 11-bit, two's complement mantissa

E is the 5-bit, two's complement exponent

PMBus™ Command set:

Command	Hex Code	Data Byte	Function
Operation	01	1	Output ON/OFF
ON_OFF_config	02	1	09, output ON default
Clear_faults	03	0	Clear Status
Write_protect	10	1	Write control
Store_default_all	11	0	Store permanently
Restore_default_all	12	0	Reset defaults
Capability	19	1	30h, 400kHz, SMBAlert
Vout_mode	20	1	Vout constants
Vout_command	21	2	Set Vout
Vout_OV_fault_limit	40	2	Set OV fault limit
Vout_OV_fault_response	41	1	
Vout_OV_warn_limit	42	2	Set OV warn limit
Vout_UV_warn_limit	43	2	Set UV warn limit
Vout_UV_fault_limit	44	2	
Vout_UV_fault_response	45	1	
Iout_OC_fault_limit	46	2	
Iout_OC_fault_response	47	1	Latch or hiccup
Iout_OC_warn_limit	4A	2	Set OC warn limit
OT_fault_limit	4F	2	
OT_fault_response	50	1	Latch or hiccup
OT_warn_limit	51	2	Set OT warn limit
UT_warn_limit	52	2	
UT_fault_limit	53	2	
UT_fault_response	54	1	
Vin_OV_fault_limit	55	2	
Vin_OV_warn_limit	57	2	Set OV warn limit
Vin_UV_warn_limit	58	2	Set UV warn limit
Vin_UV_fault_limit	59	2	Set UV shutdown
Status_byte	78	1	
Status_word	79	2	
Status_Vout	7A	1	
Status_Iout	7B	1	
Status_input	7C	1	
Status_temperature	7D	1	

Command	Hex Code	Data Field	Function
Status_CML	7E	1	
Status_other	7F	1	
Status_mfr_specific	**80**	**1**	
Status_fan_1_2	81	1	
Read_Vin	88	2	Read input voltage
Read_Vout	8B	2	Read output voltage
Read_Iout	8C	2	Read output current
Read_temperature	8D	2	Read Temperature
Read_fan_speed_1	90	2	In RPM
Read_fan_speed_2	91	2	In RPM
Read_Pout	96	2	
Read_Pin	97	2	
PMBus revision	98	1	
Mfr_ID	99	5	FRU_ID
Mfr_model	9A	15	
Mfr_revision	9B	4	
Mfr_location	9C	4	
Mfr_date	9D	6	
Mfr_serial	9E	15	
Mfr_Vin_min	A0	2	36V (linear format)
Mfr_Vin_max	A1	2	75V (linear format)
Mfr_Iin_max	A2	2	27A (linear format)
Mfr_Pin_max	A3	2	950W (linear format)
Mfr_Vout_min	A4	2	10V (linear format)
Mfr_Vout_max	A5	2	15V (linear format)
Mfr_Iout_max	A6	2	71A (linear format)
Mfr_Pout_max	A7	2	850W (linear format)
Mfr_Tambient_max	A8	2	70C (linear format)
Mfr_Tambient_min	A9	2	-10C (linear format)
User_data_00	B0	48	User memory space
User_data_01	B1	48	User memory space
FRW_revision	D0	1	
Ilimit_control_I²C	D3	2	Ilimit set (1/100A)
Vout_control_ I²C	D4	2	Vout set (1/512V)
Fan_duty_cycle	D6	1	Duty_cycle in %
Fan_speed	D7	1	Control in duty cycle
Vprog_ext	D8	2	
Read_Vout_ I²C	E0	2	1/512V
Read_Iout_ I²C	E1	2	1/100A
Read_TS_ I²C	E2	2	Heat sink temp °C
CMD_OFF_ I²C	E3	2	01-OFF, 00-ON
OTF_limit_ I²C	E4	2	OT fault limit °C
OTF_recovery_ I²C	E5	2	OT fault recovery °C
DCOKHI_ I²C	E6	2	High OV fault (1/512V)
DCOKLO_ I²C	E7	2	Low OV fault (1/512V)
Fan1_speed_ I²C	E9	2	RPM
Fan2_speed_ I2C	EA	2	RPM
Read_Vin_ I²C	ED	2	Vin (1/100V)
Read_Iin_ I²C	EE	2	Iin (1/100A)
Read_Pin_ I²C	EF	2	

Status Register Bit Allocation:

Register	Hex Code	Data Byte	Function
Status_Byte	78	7	Busy
		6	DC_ OFF
		5	Output OV Fault detected
		4	Output OC Fault detected
		3	Input UV Fault detected
		2	Temp Fault/warning detected
		1	CML (communication fault) detected
		0	None of Below
Status_word (includes Status_byte)	79	7	OV Fault/Warning detected
		6	OC Fault/Warning detected
		5	Input Fault/Warning detected
		4	Mfr_specific register change detected
		3	DC_OFF
		2	Fan Fault or Warning detected
		1	Other fault
		0	Unknown
Status_Vout	7A	7	Vout OV Fault
		6	Vout OV Warning
		5	Vout UV Warning
		4	Vout UV Fault
		3	N/A
		2	N/A
		1	N/A
		0	N/A
Status_Iout	7B	7	IOUT OC Fault
		6	N/A
		5	IOUT OC Warning
		4	N/A
		3	N/A
		2	N/A
		1	N/A
		0	N/A
Status_input	7C	7	Vin OV Fault
		6	Vin OV Warning
		5	Vin UV Warning
		4	Vin UV Fault
		3	N/A
		2	N/A
		1	N/A
		0	N/A
Status_temperature	7D	7	OT Fault
		6	OT Warning
		5	N/A
		4	N/A
		3	N/A
		2	N/A
		1	N/A
		0	N /A
Status_cml	7E	7	Invalid/Unsupported Command
		6	Invalid/Unsupported Data
		5	Packet Error Check Failed
		4	Memory Fault Detected
		3	Processor Fault Detected
		2	Reserved
		1	Other Communications Fault
		0	Other Memory or Logic Fault

Register	Hex Code	Data Byte	Function
Status_mfr_specific	80	7	3.3V_fault
		6	N/A
		5	Interrupt
		4	Fault detected
		3	PS_remote_OFF
		2	DC_fault
		1	INPUT_fault
		0	N/A
Status_fan_1_2	81	7	Fan 1 Fault
		6	Fan 2 Fault
		5	N/A
		4	N/A
		3	Fan 1 Speed Overridden
		2	Fan 2 Speed Overridden
		1	N/A
		0	N/A

Command Descriptions

Operation (01) : By default the Power supply is turned **ON** at power up as long as *Power ON/OFF* signal pin is active HI. The Operation command is used to turn the Power Supply ON or OFF via the PMBus. The data byte below follows the OPERATION command.

FUNCTION	DATA BYTE
Unit ON	80
Unit OFF	00

To **RESET** the power supply cycle the power supply OFF, wait at least 2 seconds, and then turn back ON. All alarms and shutdowns are cleared during a restart.

Clear_faults (03): This command clears all STATUS and FAULT registers and resets the SMBAlert# line.

If a fault still persists after the issuance of the clear_faults command the specific registers indicating the fault are reset and the SMBAlert# line is activated again.

WRITE_PROTECT register (10): Used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. All supported command parameters may have their parameters read, regardless of the write_protect settings. The contents of this register can be stored to non-volatile memory using the Store_default_code command. The default setting of this register is disable_all_writes except write_protect 0x80h.

FUNCTION	DATA BYTE
Enable all writes	00
Disable all writes except write_protect	80
Disable all writes except write_protect and OPERATION	40

Vout_Command (21) : This command is used to change the output voltage of the power supply. Changing the output voltage should be performed simultaneously to all power supplies operating in parallel using the Global Address (Broadcast) feature. If only a single power supply is instructed to change its output, it may attempt to source all the required power which can cause either a power limit or shutdown condition.

Software programming of output voltage permanently overrides the set point voltage configured by the **Vprog** signal pin. The program no longer looks at the '**Vprog** pin' and will not respond to any hardware voltage settings. If power is removed from the µController it will reset itself into its default configuration looking at the **Vprog** signal for output voltage control. In many applications, the **Vprog** pin is used for setting initial conditions, if different that the factory setting. Software programming then takes over once I^{2}C communications are established.

Vout_OV_warn_limit (42): **OV_warning** is extremely useful because it gives the system controller a heads up that the output voltage is drifting out of regulation and the power supply is close to shutting down. Pre-amative action may be taken before the power supply would shut down and potentially disable the system.

OC and OT_fault_ response (47, 50): The default response for both OC and OT is auto_restart (hiccup). Each register, individually, can be reconfigured into a latched state. Latched and hiccup are the only supported states.

Restart after a latch off: Either of four restart possibilities are available. The hardware pin **Remote ON/OFF** may be turned OFF and then ON**.** The unit may be commanded to restart via i2c through the *Operation* command by first turning OFF then turning ON . The third way to restart is to remove and reinsert the unit. The fourth way is to turn OFF and then turn ON ac power to the unit. The fifth way is by changing firmware from **latch off** to **restart.** Each of these commands must keep the power supply in the OFF state for at least 2 seconds, with the exception of changing to **restart**.

A power system that is comprised of a number of power supplies could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual power supplies. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by;

1. Issuing a GLOBAL OFF and then ON command to all power supplies,
2. Toggling Off and then ON the **Remote ON/OFF** signal
3. Removing and reapplying input commercial power to the entire system.

The power supplies should be turned OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual power supplies.

Auto_restart: Auto-restart is the default configuration for recovering from over-current and over-temperature shutdowns.

An overvoltage shutdown is followed by three attempted restarts, each restart delayed 1 second, within a 1 minute window. If within the 1 minute window three attempted restarts failed, the unit will latch OFF. If less than 3 shutdowns occur within the 1 minute window then the count for latch OFF resets and the 1 minute window starts all over again.

Vin_UV_warn_limit (58): This is another warning flag indicating that the input voltage is decreasing dangerously close to the low input voltage shutdown level.

Status_word (79): returns two bytes of information. The upper byte bit functionality is tabulated in the Status_word section. The lower byte bit functionality is identical to Status_byte.

Fan_speed (D7): This register can be used to 'read' the fan speed in adjustment percent (0 – 100%) or set the fan speed in adjustment percent (0 – 100%). The speed of the fan cannot be reduced below what the power supply requires for its operation. The register value is the percent number, it is not in linear format.

Invalid commands or data: The power supply notifies the MASTER if a non-supported command has been sent or invalid data has been received. Notification is implemented by setting the appropriate STATUS and ALARM registers and setting the SMBAlert# flag.

Control and Read accuracy:

The estimates below are believed to be reasonable under most operating conditions. However, these are typical numbers and not hard bound values that cannot be exceeded. In most nominal operating conditions the returned values are significantly better than these estimates.

FUNCTION	ACCURACY
Vout_command	± 2%
Vout_OV_fault_limit	± 3%
Iout_OC_warn_limit	± 4% of FL
OT_warn_limit	± 5°C
Vin_UV_warn_limit	± 3%
Vin_UV_fault_limit	± 3%
Read_Vin	± 3%
Read_Vout	± 2%
Read_Iout	± 4% of FL
Read_temperature	± 5°C

EEPROM

The microcontroller has 96 bytes of EEPROM memory available for the system host.

A separate EEPROM IC, with write protect features, provides another 128 bytes of memory. Minimum information to be included in this separate EEPROM: model number, revision, date code, serial number etc.

LEDs

Two LEDs are located on the front faceplate. The INPUT OK LED provides visual indication of the INPUT signal function. When the LED is ON GREEN the power supply input is within normal design limits.

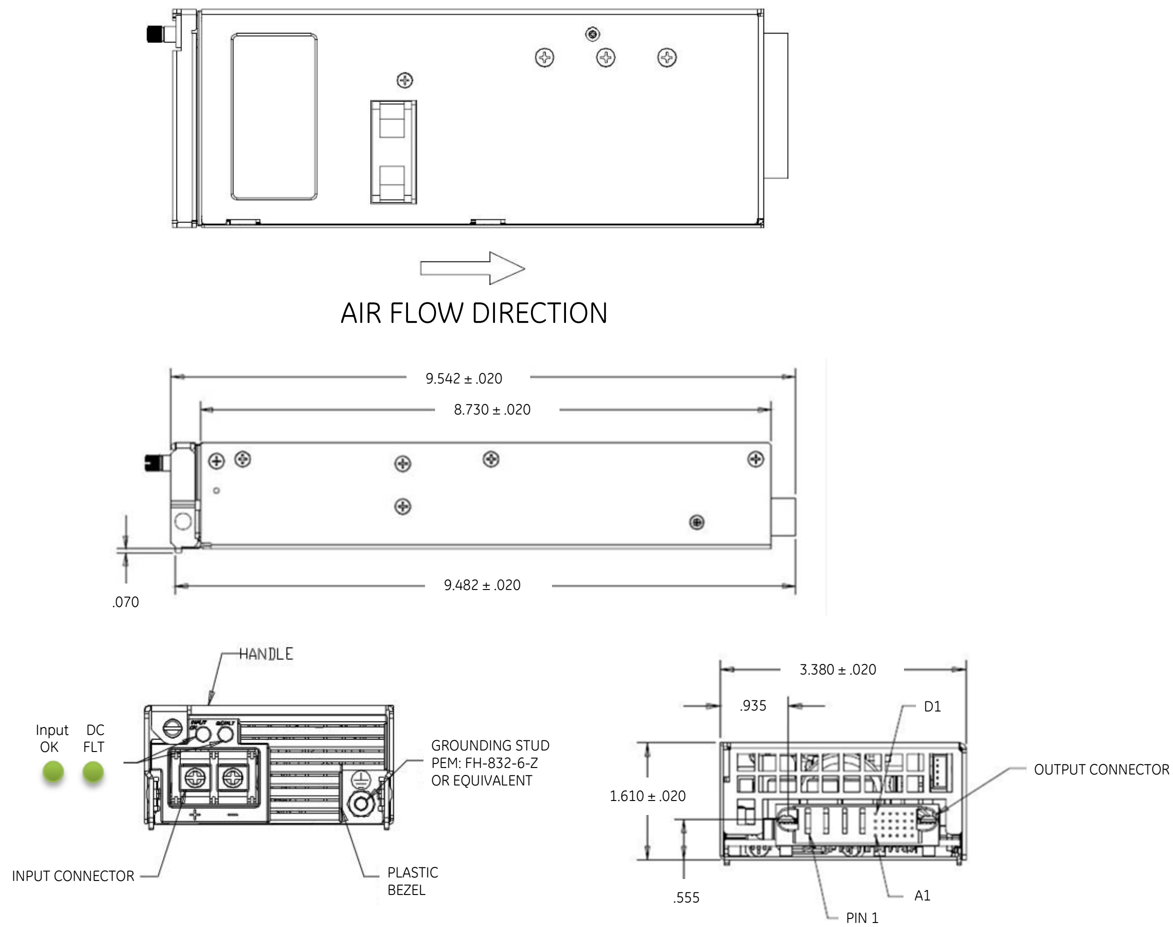
The second LED DC/FLT provides visual indication of three different states of the power supply. When the LED is GREEN then there are no faults and the DC output is present. When the LED is AMBER then a fault condition exists but the power supply still provides output power. When the LED is RED then a fault condition exists and the power supply does not provide output power.

Alarm/LED indicator Table

	Test Condition	LED Indicator		Monitoring Signals			
		LED1 INPUT OK	Tri-Color LED2 DC OK	FAULT	DC OK	INPUT OK	TEMP OK
1	Normal Operation	Green	Green	High	High	High	High
2	Low or NO INPUT	Off	Red	Low	Low	Low	High
3	OVP	Green	Red	Low	Low	High	High
4	Over Current	Green	Red	Low	Low	High	High
5	Temp Alarm Warning	Green	Orange	High	High	High	Low
6	Fault Over Temp	Green	Red	Low	Low	High	Low
7	Remote ON/OFF	Green	Red	Low	Low	High	High

Note: Test condition #2 had 2 modules plug in. One module is running and the other one is with no Input.

Outline Drawing

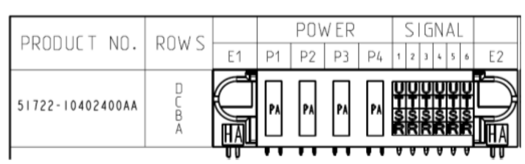


Connector Pin Assignments

Input Connector: DINKLE DT-7C-B14W-02 (see pin assignment on front face plate)

Output Connector:

FCI Berg P/N: 51732-077LF (replaces 51722-10402400ABLF)
Mating connector: FCI Berg P/N 51762-10402400ABLF



	Function	Pin	Function	Pin	Function	Pin	Function
A1	V$_{STDBY}$ [3.3V]	B1	Fault	C1	ISHARE	D1	VProg
A2	V$_{STDBY}$ [3.3V] Return	B2	I Monitor (IMON)	C2	N/C	D2	OVP Test Point
A3	Signal Return	B3	Enable	C3	Over Temp Warning	D3	Remote ON/OFF
A4	Write Protect (WP)	B4	PS Present	C4	I^{2}C Address (A0)	D4	DC OK
A5	Remote Sense (+)	B5	SDA (I^{2}C bus)	C5	I^{2}C Address (A1)	D5	INPUT OK
A6	Remote Sense (-)	B6	SCL (I^{2}C bus)	C6	I^{2}C Address (A2)	D6	Interrupt
P1	+Vout	P2	+Vout	P3	Output Return	P4	Output Return

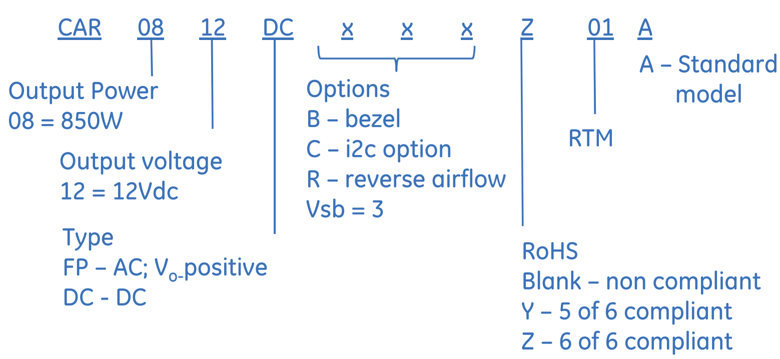
Data Sheet

Ordering Information

Please contact your GE Sales Representative for pricing, availability and optional features.

PRODUCT	DESCRIPTION	PART NUMBER
850W Front-End	+12V$_{OUT}$ Front-End w/Bezel, 3.3V$_{STDBY}$	CAR0812DCBXXZ01A
850W Front-End	+12V$_{OUT}$ Front-End w/o Bezel, 3.3V$_{STDBY}$	CAR0812DCXXXZ01A
850W Front-End	+12V$_{OUT}$ Front-End w/Bezel, 5V$_{STDBY}$	CAR0812DCBX5Z01A
850W Front-End	+12V$_{OUT}$ Front-End w/o Bezel, 5V$_{STDBY}$	CAR0812DCXX5Z01A

PART NUMBER DEFINITION GUIDE EXAMPLE



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